Summary of the First IEEE Silicon Debug & Diagnosis Workshop 2004

Fidel Muradali, Program Chair

Debug looks into what to do when a circuit does not behave as intended. It is a requirement in the modern product creation flow. Unfortunately, processes related to debug and diagnosis can become unpredictably expensive time sinks. As a result, the IEEE Silicon Debug and Diagnosis (SDD) Workshop was created to find solutions and promote the exchange of practical ideas in this area.

The first SDD Workshop was held in conjunction with the European Test Symposium at the Ajaccio Convention Center, Corsica, France on May 26th-27th. . The workshop was well attended – 36 participants from fields including semiconductor and electronic system manufacturers, IP providers, test and measurement, EDA and advanced research labs. The audience possessed broad practical interests. These included prototype turn-on, diagnostic flows, silicon editing, on-chip design for debug and test quality improvement

The format of the Workshop was a one and a half day discussion forum guided by papers, panels and audience comments. After opening with a tutorial on debug and diagnosis fundamentals, the Workshop quickly centered on defining the SDD problem space and aligning the terminology used by the diverse participants.

Papers and discussions probed for a 'wish list' of items that a debug and diagnosis portfolio should contain. Fundamentally, it was agreed that the acceptability afforded to design for testability should extend to debug and diagnosis. That is, we need to move beyond the pass/fail manufacturing test philosophy towards providing control and observe to integrated circuits for purposes of debug. For instance, provide the ability to "poke around" the chip during turn-on similar to the way one manipulates simulation. The ability to logically control clocking, change selected state variables, perform experiments based on user-defined triggers or internal flags, perform timing-oriented measurements and quickly extract/capture circuit states while preserving the functional sequence would all aid in achieving this objective.

Debug and diagnosis provide information needed to fix the circuit, fix the test environment, fix test program quality, fix the fabrication process, … *fix something*. In order to gather such information, examples of on-chip and in-system monitoring were presented. The use of ATE (both conventional testers and DFT testers) for data gathering and scan-based debug was also discussed.

Of course, these are just the tip of the iceberg – a number of shortcomings exist in technology. SDD is not yet as formalized and commercialized as well-known structural testing. Tools, techniques, usable equipment and data are all open issues. As many of the structures and approaches require functional circuit information, an appropriate communication model, documentation and problem ownership must exist between people designing the circuit and those performing the debug/diagnosis tasks. It is well known that in a contemporary environment, these parties may be distributed globally and/or outsourced. Even when debug is successful, the error must be reproducible on a manufacturing platform (the platform itself must be set up so that it does not introduce false failures). Further, as discussed in presentations on new silicon editing techniques (e.g. focused ion beam and laser stimulation) a logical 'root cause' is typically confirmed via expensive physical techniques. The business model for this in a disaggregated supply chain could be an opportunity.

The next SDD Workshop is currently being planned. It is expected that emphasis will be placed on examples and case studies. The working group of participants will continue to explore the SDD issue and select topics for greater focus. Potential areas for standardization will also be evaluated.