

IEEE International Silicon Debug & Diagnosis Workshop 2005
November 10th - 11th

<http://evia.ucsd.edu/conferences/sdd/05/index.html>

Day 1 - November 10th

4:00pm – Opening Remarks – Mike Ricchetti, ATI, Fidel Muradali,
4:15pm – 4:45 pm – Silicon-Debug Challenges vs. Silicon-Aware IP – *Yervant Zorian, Virage Logic*
<15min break>

Session 1 – 5:00pm – 6:30pm

Moderator – Fidel Muradali

Terminology Update – *Miron Abramovici, DAFCA*

Role of Circuit Edit in Post-Silicon Debug and Diagnostics – *Tahir Malik, Rajesh Jain, Roger Nicholson, Ted. Lundquist, Credence Systems*

System impact of gaps in Test & Debug – *Bill Eklow, Cisco*

Snapshot Practical Case – *Bruce Cory, Nvidia*

Snapshot Practical Case – *Rob Aitken, ARM*

7pm – 9pm Welcome reception

Day 2 – November 11th

Session 2: Debug Examples

Moderator – Chinsong Sul, Silicon Image

8:00am – 9:45am

Snapshot Practical Case – *Doug Josephson, Intel*

Case Studies in Debug of subtle ASIC Design Problems - *Pamela Gillis, Tad Wilder, IBM*

A Diagnosis Oriented Proactive-DFM Technique - *D. Apello, V. Tancorre - ST. Microelectronics; P. Bernardi, M. Grosso, M. Rebauendgo, M. Sonza Reorda – Politecnico di Torino*

A New Approach to Silicon Debug – *Miron Abramovici, DAFCA; Yu-Chin Hsu, Novas*

9:45am – 10:15am – BREAK

Session 3: Making a Better Debug/Diagnosis System

Moderator – Erik-Jan Marinissen., Philips

10:15am – 12:00am

Discussion (80min): Address the gaps in the papers of Session 1.

- Precisely what would be needed to make process easier?
- From the learning, what preventative DFD/DFT/Procedure can be done for the future?
- Identify other practical gaps suggested from audience experience.
- What is needed & feasible from ATE, EDA, IP, Customers, suppliers, standards, etc.
- Impact of particular environment (e.g. Fabless, cross-geography, tooling).
- What tools & environment was like 5 yrs ago vs. today vs. 2 yrs from now. Realistically, what can and cannot be done in 2yrs ... 5yrs

Program

In conjunction with the International Test Conference'05

Paper: X-Fault Model Based Diagnosis – *Yu Huang, W-T Cheng - Mentor Graphics; Zhiyuan Wang-Cisco*

LUNCH - 12:00 pm – 1:00pm

Session 4: Short Diagnosis talks (15min each + 5min Q/A)

Moderator – Rob Aitken, ARM

1:00pm - 2:20pm

Snapshot Practical Case – Shrikanth Venkataraman, Intel

Diagnosis of Defects on Scan Enable Trees – Yu Huang, Mentor Graphics; Keith Gallie-LSI

Debugging AC Lbist – Nikhil Dakwala, Stridge Inc.

Post-BIST Fault Diagnosis for Multiple Stuck-at Faults – Hiroshi Takahashi, Yukihiro Yamamoto, Yoshinobu Higami, Yuzo Takamatsu – Ehime University; Koji Yamazaki – Meji University; Takashi Aikyo – Fujitsu; Yasuo Sato - STARC

<Break>

Session 5: In-situ System Debug – Interface to IEEE Standards

Moderator – Neal Stollon., First Silicon Solutions

2:30pm – 4:00pm

Optimized JTAG interface - Lee Whetsel, Texas Instruments

Discussion: (60 min)

Discuss possible extensions, tooling and open issues related to interfacing a mature standard to a debug/diagnosis environment. The initial objective of these standards may have been specific to an issue other than debug/diagnosis (e.g. JTAG was intended for test).

Overview progress of current DFD consortium.

4:00pm – 4:15pm : Closing remarks

6:00pm – Social